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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/870,447	06/01/2001	Brian Boles	18153.0045	8455

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BAKER BOTTS L.L.P.  
PATENT DEPARTMENT  
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AUSTIN, TX 78701-4039

EXAMINER

CLEARY, THOMAS J

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Serial No. : 09870447  
Applicant : Brian Boles  
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Date Mailed : November 10, 2005

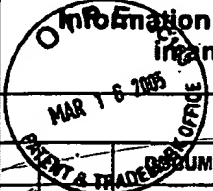
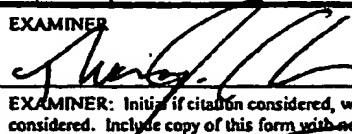
## ACKNOWLEDGEMENT OF REQUEST

### *Notice of Allowance/Allowability Mailed*

The request for a copy of the initialed PTO 1449, dated December 10, 2004, has been received by the U.S. Patent and Trademark Office.

- Requested copy attached

SUNDA M. ARCHER  
For the Office of Patent Publication

PTO-1449		Application No. 09/870,447		Applicant(s) Brian Boles et al.		
<b>Information Disclosure Citation</b> <b>Iran Application</b> 		Docket Number 068354.1471		Group Art Unit 2111	Filing Date June 1, 2001	
		<b>U.S. PATENT DOCUMENTS</b>				
	DOCUMENT NO.	DATE	NAME	CLASS	SUBCLASS	FILING DATE
<del>TS</del> A.	3930253	12/30/75	Maida	340	347	1/24/74
<del>TS</del> B.	5974549	10/26/99	Golan	713	200	3/27/97
<del>TS</del> C.	6055619	4/25/00	North et al.	713	36	2/7/97
<del>TS</del> D.	6282637	8/28/01	Chan et al.	712	223	12/2/98
<del>TS</del> E.	6728856	4/27/04	Grosbach et al.	711	202	6/1/01
F.						
G.						
H.						
I.						
J.						
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	DOCUMENT NO.	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES NO
<del>TS</del> K.	01037424 A	2/89	JP	H03M	001/82	X
<del>TS</del> L.	0 554 917 A2	8/11/93	EP	G06F	9/26	X
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EXAMINER 				DATE CONSIDERED 10-June-05		
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